A 12-Bit High-Speed Column-Parallel Two-Stage Pipelined SAR Analog-to-Digital Converter for CMOS Image Sensors

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***Abstract*—A 12-b column-parallel high-speed area-efficient pipelined SAR analog-to-digital converter (ADC) for CMOS image sensors (CIS) is proposed in this paper. The two-stage pipelined SAR are implemented into a 5-um-pitch column. The proposed structure achieves a reduction in the number of capacitors used, which is the dominant area and power consumer in SAR ADC. The prototype was designed in a 65 nm CMOS process with an active area of 0.0054 mm2. The ADC achieves 1 usec conversion time and consumes less than 125 uW, enabling a high speed and area-efficient column-parallel imagining array.**

***Index Terms*—ADC, analog to digital convertor, pipelined SAR ADC, SAR ADC, pipelined ADC, CMOS image sensors, column-parallel.**

I. Introduction

Many imager applications require high-speed video and high-resolution high-speed CMOS image sensors (CIS). For large frames and relatively high-pixel rate, state of the art CIS uses column-parallel Analog-to-Digital Conversion (ADC) channels. The imager frame rate is typically limited by the ADC speed. Therefore, high speed ADCs are required for such high frame rate CIS.

Slope ADC is the most popular and leading architecture for CIS. Moreover, Successive Approximation Register (SAR) and Cyclic ADC have been often proposed for Slope ADC replacement [1] [2]. Slope ADC is very compact and power efficient, however it requires 2^N clock cycles for N bit conversion, therefore is not appropriate for high speed.

Cyclic ADCs provide higher speed compared to slope ADC as only N clock cycles are required for bit conversion. However, they require high power-consuming operational amplifiers.

In communication channels and many other applications the SAR ADC architecture is known for its excellent power efficiency in moderate resolutions [3]. It is also very suitable for advanced CMOS process due to the low number of analog components required. However, it is usually restricted in speed due to the serial successive approximation process that requires N clock cycles and in resolution due to comparator noise and capacitor matching requirements. On top of that, when trying to use the SAR ADC in high-resolution designs, the input capacitance gets large due to the minimum unit capacitor size required for sufficient matching, consequently consuming high power and losing its attractiveness.

Pipelined ADC architecture on the other hand, can help achieve both high speed and resolution, but as the cost of power-hungry high-gain high-bandwidth amplifiers, as well as power and area consuming Flash sub-ADC.

One method to overcome those issues is by replacing the conventional Flash sub-ADC with SAR [4]. The so-called pipelined SAR ADC combines the advantages of pipelined and SAR ADCs and can acquire good tradeoffs of power, area, resolution, and sampling rate. This hybrid architecture quantizes the analog stage by stage like the conventional pipelined ADC. The SAR ADC composing each stage has a decreased conversion time due to lower resolution.

In this work a column-parallel pipelined SAR ADC aimed at CIS is presented. As compared to moderate resolution SAR ADCs of 9-11b which spend a considerable amount of time due to the serial decision process, both sub-ADC stages in this work are rather low-resolution SAR ADCs of 6-7-bit. A larger unit capacitor can be used with sufficient matching, therefore relaxing any need for capacitor mismatch calibration. The pipelined SAR ADC also eliminates the need for an active front-end S/H circuit as in the conventional pipelined ADC because the sub-ADC and sub-DAC share the same sampling path.

This pipelined SAR ADC proposed in this work is composed of a large first-stage 6-bit SAR ADC based Multiplying

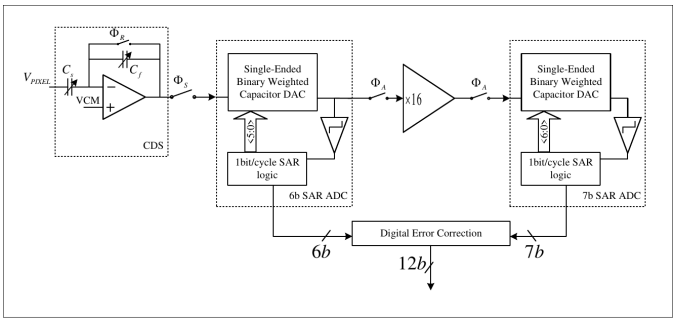

Fig. 1. Architecture of the proposed 12b 1MS/s Pipelined SAR ADC.

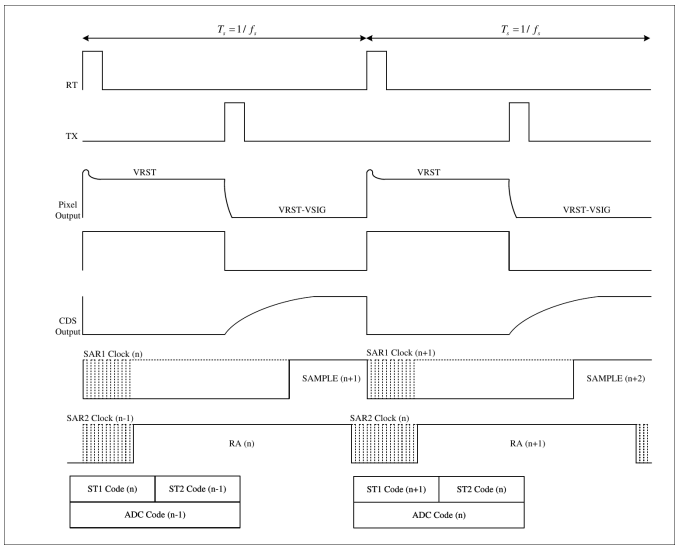

Fig. 2. Pipelined SAR ADC timing.

Digital-to-Analog convertor (MDAC) and a second stage of a 7-bit SAR ADC. The architecture achieves an optimal compromise between resolution, speed and power that is very suitable for column-parallel CIS.

Using large number of bits in the first stage reduces the sensitivity to errors and noise in the following stage. A few low-power techniques are utilized in this work. The first stage MDAC gain is halved to allow the residual amplifier to use less current for the same settling demands and to relax to open-loop gain and output voltage swing. One bit of redundancy is used to facilitate digital error correction (DEC) of the first stage sub-ADC, allowing it relaxed requirements and hence power reduction in the comparator.

II. ADC ARCHITECTURE

Fig. 1 shows the block diagram of the 12-bit pipelined SAR ADC. The resolution for the first and second stage of the sub-ADCs are $N_1 = 6$ bits and $N_2 = 7$ bits, respectively. The total ADC resolution is given by $N = N_1 + N_2 - 1 = 12$ due to the second stage's 1-bit redundancy for the DEC. The first stage of SAR ADC is composed of a 6-bit capacitive DAC (CDAC) which also functions as the input sampling capacitance. This last one is an advantage that reduces the area requirements and eliminates the path mismatch compared to the conventional pipelined ADC, which uses a Flash sub-ADC and an additional front-end power-hungry S/H to alleviate the path mismatch problem. The CDAC uses the 6-bit binary weighted charge redistribution architecture. Fig. 2 shows the timing diagram of the analog-to-digital conversion. RT and TX present the pixel reset and transfer control signals, respectively, used as in a regular 4T CIS pixel. Φ_R controls the reset switch of the CDS, sampling the pixel reset voltage. The CDS is based on a single-ended amplifier which cancels reset noise by subtracting the reset level from the signal level generated by the pixel. After the switch opens, the CDS cancels the reset noise in the pixel output signal. The two samples difference is then amplified and sampled by the ADC. In order to optimize the input dynamic voltage of the SAR stage, the CDS also provides the ability for a variable analog-gain (AG) using the capacitance ratio C_s/C_f.

Φ_S goes high to start the ADC sampling phase. The pipelined SAR ADC samples the analog input signal from the CDS onto the first stage CDAC and begins converting it into 12-bit digital data. The first stage quantizes the input using SAR algorithm into a 6-bit digital word triggered by the SAR1 CLK. At the end of the SAR conversion, a residue is generated at the top plate of the first stage CDAC. This residue is the difference between the analog input and the quantized analog input provided by the DAC.

The amplifier, which is based on capacitive feedback provides the residue amplification between both stages. The closed-loop gain of the amplifier is reduced in a factor of two to avoid the output going above the permitted voltage dynamic range of the next stage. During RA phase, Φ_A goes high, allowing amplification of the residual while the second stage samples it on its CDAC. After the amplification phase is done, the second stage will convert the input into a 7b digital word. The second stage SAR ADC samples the residue amplifier output voltage and quantizes it to a 7b fine code, triggered by the SAR2 CLK. To optimize area and increase speed, the second stage works concurrently with the first stage which is now in the sampling phase starting a new quantization cycle. The two digital codes from both stages enter the DEC logic to code the final 12-bit output code.

In a conventional pipelined ADC, a known method to prevent data loss in the pipelined stages is by using the 1.5-bit redundancy technique. It is done by generating offsets into the sub-DAC and sub-ADC and removing the top comparator from the 2-bit regular stage topology. In a pipelined SAR ADC, it should take extra time and circuit complexity to use the above method. In this work, an offset of 0.5·LSB of the first stage resolution is generated into the CDAC. This offset generates offset in both the sub-DAC and the sub-ADC at once, allowing the DEC mechanism to use addition-only error correction, preventing complex digital circuitry in the DEC block. The DEC corrects the digital codes from both stages by overlapping one bit between them.

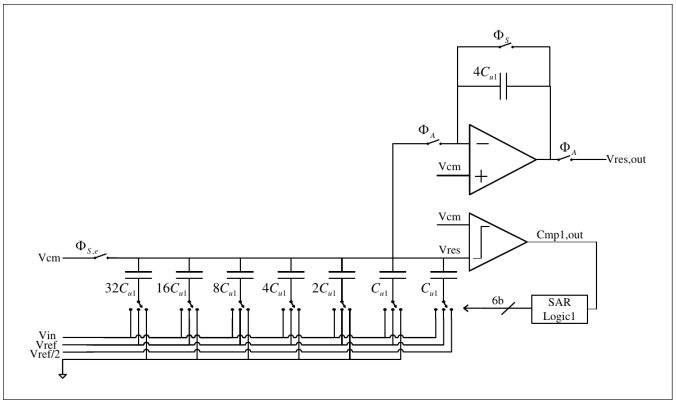

Fig. 3. First stage 6-bit SAR ADC and Residual Amplifier.

III. Circuit implementation

A. First stage 6-bit SAR ADC

Fig. 3 shows the block diagram of the first stage SAR ADC composed of 64-unit Metal-Insulator-Metal (MIM) capacitors and a comparator. It also shows the Residual Amplifier. The analog input signal is implemented using bottom plate sampling technique to ensure high accuracy while Φ_S is high. $\Phi_{S,e}$ will go low at the end of the sampling phase, canceling charge injection effects. The SAR algorithm will begin by connecting the bottom plate of the MSB capacitor $32C_{u1}$ to the reference voltage Vref. SAR CLK1 will strobe the comparator to execute the first decision with the CLK falling edge. The SAR conversion will continue in the familiar method until it quantizes the input into a 6-bit digital word.

The first stage CDAC is also used as the input sampling capacitor, eliminating the need for a big power-hungry front-end active S/H. The value of the first stage CDAC unit capacitor is 44.13 fF occupying an area of 2.9×2.9 μm^2 , resulting in a total sampling capacitance of 2.82 pF. This value meets by far the demand for the KT/C noise and capacitor matching. The choice for the minimal unit capacitor value is due to process constraints.

Capacitor matching dominates the static linearity errors of the SAR ADC. The maximum error in a conventional binary-weighted CDAC occurs on the MSB code transition where the entire capacitor's array switches states from '1000…0' to '0111…1'.

The worst-case DNL for the first stage:

$$\sigma_{DNL_1,MAX} = \sqrt{2^{N_1}-1}\cdot\sigma_{C_{u1}}\cdot V_{LSB_1}/C_{u,mm} \quad (1)$$

$\sigma_{C_{u1}}$ is the standard deviation of the unit capacitor and C_{u1} is the unit capacitor value of the first stage. The accuracy of the first stage DNL must meet the entire ADC resolution, therefore yielding the next mismatch constraint:

$$6\cdot 2^{N-N_1}\sqrt{2^{N_1}-1}\cdot\sigma_{C_{u1}} < C_{u,mm} \quad (2)$$

The thermal noise of the first stage input sampling capacitor should be lower than the full ADC resolution quantization error $q_n^2 = V_{LSB}^2/12 = \left(V_{FS}/2^N\right)^2/12$, providing the thermal noise constraint:

$$12kT\cdot 2^{2N-N_1}/V_{FS}^2 \le C_{u,th} \quad (3)$$

V_{FS} is the ADC input full-scale voltage, k is the Boltzmann constant and T is the absolute temperature. The unit capacitor will be sized as the $\max\{C_{u,th}, C_{u,mm}, C_{u,pr}\}$, $C_{u,pr}$ being the process limited capacitor value.

The dynamic latch comparator used in the ADC. The comparator is without a pre-amplifier stage due to the relaxed constraints of using a low-resolution stage, allowing power saving.

B. Residue Amplifier

The residue amplifier is designed for high open-loop gain and bandwidth to meet accuracy constraints [5]. In the sampling phase, while Φ_S is high, the residual amplifier resets the feedback capacitor C_f using negative feedback. In the amplification phase, when Φ_A is high, the feedback capacitor is getting out of reset, amplifying the first stage residual by a closed-loop gain of $A_{CL} = C_{DAC_1}/C_f$.

In a conventional pipelined stage, the amplifier closed-loop gain is 2^{N_1-1-M}, where M is the gain reduction parameter. This paper utilizes the "half-gain" technique [2] to halve the MDAC gain from the conventional approach $2^{N_1-1} = 32$ (M=0), to $2^{N_1-2} = 16$ (M=1). This technique, while using M=1, results in a double closed-loop bandwidth for the same current consumption. Consequently, the power consumption can be reduced by half for the same settling error. Usage of a higher gain reduction parameter will require more sampling capacitance in the second CDAC for the same thermal noise constraints.

The amplification error is generated by both static and dynamic errors. A budget of half an error for the static and half for the dynamic yield the following constraints:

$$V_{in,st2} = \underbrace{V_{residual}\cdot G}_{ideal} + \underbrace{V_{residual}\cdot G\cdot\varepsilon_{static}}_{error} \quad (4)$$

$$V_{residual}\cdot G\cdot\varepsilon_{static} \le \frac{1}{4}\cdot V_{FS}/2^{N-N_1+M} \quad (5)$$

$$A_{OL} \ge 2^{N-M} \quad (6)$$

$$\varepsilon_{dynamic} = e^{-\frac{t}{\tau_s}} = e^{-t\cdot\beta\cdot\omega_{GBW}} \le \frac{1}{4}\cdot V_{FS}/2^{N-N_1+M} \quad (7)$$

$$f_{GBW,\min} \ge [N+2-N_1+M]\cdot\ln(2)\cdot 2^{N_1-1-M}/(2\pi\cdot t_{RA}) \quad (8)$$

Where A_{OL} is the amplifier's open-loop gain, β is the feedback factor, f_{GBW} is the amplifier's unity gain frequency and t_{RA} is the time allocated for residual amplification.

In addition, the output swing of the amplifier is also reduced by half, allowing it to cascade more devices for enhanced gain. The op-amp has a low output single-ended peak-to-peak swing requirement of only $V_{swing,SE} = 2\frac{V_{ref}}{2^{N_1}}\cdot 2^{N_1-1-M} = \frac{V_{ref}}{2^M}$.

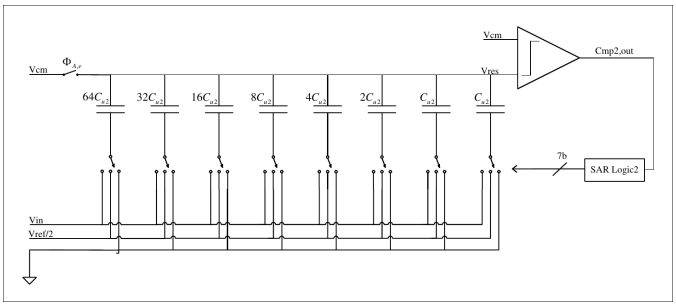

Fig. 4. Second stage 7-bit SAR ADC.

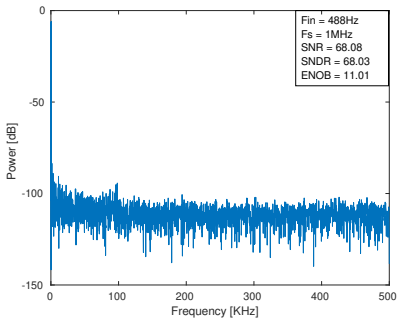

Fig. 5. 4096 point FFT for 488 Hz input.

C. Second-stage 7-bit SAR ADC

Fig. 4 shows the second stage of 7-bit SAR ADC.

The second stage will quantize its input while comparing it to half the full-scale reference voltage due to the half-gain technique, hence needs to meet the accuracy requirements of 8b ADC with a full-scale signal range.

The errors and noise occurring in the second stage are almost eliminated by the large gain of the amplifier, relaxing the constraints of the second stage noise and accuracy significantly. Therefore, excessive capacitive load and consequent power consumption can be eliminated. The Striped Stacked Metal Capacitor used for the second stage CDAC is only 3.746 fF and occupies an area of 9.2 μm^2, yielding a total sampling capacitance of 480 fF.

The second stage dynamic latch comparator is very similar to the dynamic latch used in the first stage but optimized for low noise, trading it for speed.

IV. Measurement Results

The prototype Pipelined SAR ADC was designed using ST65 nm CMOS process. The ADC occupies a core area of 5400 μm^2 and is implemented in a 5 μm pitch aimed at column-parallel operation. The resulting height of the ADC column-parallel channels is approximately 1 mm and is driven by dedicated periphery circuits. The ADC is used under a dual-supply mode. With supply voltage of $V_{DD} = 2V$ for the OTA and $V_{DD} = 1.2V$ for the remaining circuitry, the ADC draws 122.3 μW. The residual amplifier consumes 108.6 μW, almost 90% of the total ADC power which is due to the static currents flowing in the OTA even in idle.

Fig. 5 shows the simulated 4096-point FFT spectrum of the pipelined SAR ADC with a sampling rate of 1MS/s with near-DC input tone (488Hz). The SNDR, SNR and ENOB are 68.03 dB, 68.08 dB and 11.01, respectively. The performance of the ADC is summarized in table I.

The performance of the proposed pipelined SAR ADC is compared with the state-of-the-art ADCs in table II. For various FoMs, the prototype CIS demonstrates state-of-the-art level performances.

V. Conclusion

This paper has presented a 12-bit 1MS/s area-efficient pipelined SAR ADC for high-speed CIS. This work exploits low power design strategy imposing maximum simplicity on ADC circuitry. The 12-bit ADC is divided into large 6-bit first-stage SAR ADC and 7-bit second-stage SAR ADC. The prototype implemented in 65 nm CMOS process occupies 5400 μm^2 and dissipates 122.3 μW at a conversion speed of 1μ sec and readout noise of 301.23 $\mu Vrms$. The prototype ADC demonstrates the ability of this architecture and its usage in high-speed CIS with a small pixel pitch.

TABLE I
Summary of ADC Performance

Process	65 nm CMOS
Pitch	5 μm
Core Area	5400 μm^2
ADC Resolution	12-bit
Conversion Time	1 μsec
Conversion Rate	1 MHz
Input Range	1 V
Supply Voltage	2 V (Analog) 1.2 V (Digital)
Power Consumption	122.3 μW
SNR	68.08 dB
SNDR	68.03 dB
ENOB	11.01 dB
Readout Noise (AG = 1)	301.23 $\mu Vrms$
Dynamic Range	70.42 dB
$*FoM_1$	45.08 fJ/conversion-step
$**FoM_2$	0.089 fJ·μm^2/conversion-step

$*FoM_1 = P/f_s \cdot 2^{ENOB}$

$**FoM_2 = P \cdot T_{conv} \cdot A/10^{\frac{DR_{dB}-1.76}{10}}$ [10]

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TABLE II
Comparison of ADCs for Image Sensors

Reference	[9]	[1]	[8]	[7]	[2]	[6]	This Work
Architecture	SS-FTDC	SAR	SAR	Cyclic-Cyclic	Cyclic-Cyclic	Cyclic-Cyclic-SAR	Pipelined SAR
Resolution [bit]	12	14	10	14	12	12	12
Conversion time [usec]	1	1.7	1.78	1.85	1.92	0.92	1
Pitch [μm]	5.6	8.4	9	6.4	5.6	4.4	5
Area [μm^2]	-	11088	3825	12113	9912	4048	5400
Power [μW]	177	41	41	120	101	120	122.3
Readout Noise (AG=1) [$\mu Vrms$]	45.08	1000	2373	411	321.3	414	301.23
Dynamic Range [dB]	66.43	60.00	52.49	67.72	69.86	67.66	70.42
$*FoM_1$	103.32	85.3	211.96	111.65	76.24	55.93	45.08
FoM_2	-	1.16	2.36	0.68	0.298	0.1149	0.09

FoM_1 by Walden is based on DR and not the conventional SNDR

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